

DATA TRANSITION IDENTIFIER

Abstract of the Disclosure

The invention relates to methods and apparatus that indicate a first logic state and a second logic state associated with consecutive bits in a serial bitstream of a relatively high-frequency network. The serial bitstream is demultiplexed to retrieve the consecutive bits, and the consecutive bits are provided as inputs to an identifier circuit. The identifier circuit receives the demultiplexed consecutive bits and indicates via balanced outputs whether consecutive bits of the serial bitstream corresponded to logic 0 to logic 0, logic 0 to logic 1, logic 1 to logic 0, or logic 1 to logic 1. The balanced outputs that indicate the logic 0 to logic 0 sequence, the logic 0 to logic 1 sequence, the logic 1 to logic 0 sequence, and the logic 1 to logic 1 sequence advantageously provide matched delays from an activation of the identifier circuit to the activation of one of the balanced outputs.